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DESIGN TECHNIQUES FOR LOW POWER VLSI DESIGN

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Abstract: ***With the advancement in VLSI technology and shrinking of the devices, power dissipation has emerged as an important factor while considering performance and area for VLSI Chip design. The need of low power VLSI design has become highly important, for portable applications. As the complexity of the chips is increasing day by day, the difficulty in limiting the power dissipation may limit the functionality of the computing systems. For the recent CMOS feature sizes, leakage power dissipation has also become an overriding feature for VLSI circuit designers. Power dissipation occurs at all the levels of abstraction like system level, architecture level, circuit level and physical level. In this paper the author has identified many low power strategies and techniques to override these difficulties.***

Keywords: **Dynamic power, Low power design, Power dissipation, VLSI.**

I. INTRODUCTION

The major concerns of the VLSI designer were area, performance, cost and reliability; power considerations were mostly of only secondary importance in last decades but in recent years power is being given comparable weight to area and speed. The optimization of a circuit for speed and power is nearly always conflicting i.e., higher speed leads to higher power dissipation and vice versa. Portable and handheld devices demand high-speed computation and complex functionality with low power consumption. For these applications, average power consumption is a very important design constraint to be considered. The power is starting to limit the speed of VLSI processors. The need for low power consumption is increasing as components are becoming battery-operated, smaller and require more functionality and features. Designers go through several iterations to optimize power in order to achieve their power budgets.

Although power is to be optimized at all levels of abstractions, optimizations in early design stages have much impact in reducing power. Because of shrinking of the devices, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths will result in increase in sub-threshold leakage current. Because of scaling, low threshold voltage also results in increase in sub-threshold leakage current because transistors cannot be turned off completely. For these reasons as mentioned, leakage power dissipation, has become a major part of total

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power consumption for VLSI technology. It is very important to choose the circuit topology that would yield desired performance for a given power budget.

Many techniques used for optimization of power are the asynchronous logic and adiabatic logic. These two technologies have been combined to create an Asynchronous, Adiabatic Logic methodology, called Asynchrobatic Logic. The basic low-power design techniques, includes clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current. At circuit level, any low power method can be used for general digital systems. There are numerous generic methods on low power design, including Power Island, Clock Gating, Transistor Resizing, Operating in sub-threshold regime, MTCMOS, VTCMOS, as well as various leakage power reduction techniques such as using Sleep Transistor, Forward/Reverse Body Biasing.

II. BASICS OF POWER DISSIPATION AND ITS CAUSES

The basic components that are responsible for power dissipation are dynamic power, short-circuit power and leakage power; $P= P_{dynamic} + P_{short\ circuit} + P_{leakage}$; from which dynamic power or switching power is nearly 90% of total power dissipation given by,

$$P_{dynamic} = C_L V_{dd}^2 \alpha \quad (1)$$

where, C_L: Load Capacitance, V_{dd}: Supply Voltage, α: Activity Factor, meaning how often, on average, the wires switch, f: Clock Frequency. The term dynamic power dissipation refers to the sum of short circuit and capacitive dissipations. $P_{shortcircuit}$ is the short circuit power which is caused due to the rise time and fall time of input signals. Short circuit power is approximately 10%-15% of the dynamic power, $P_{shortcircuit} = I_{short\ circuit} * Vdd$. However if gate sizes are selected so that the input and output rise/fall times are about equal, the short-circuit power consumption will be less than 15% of the dynamic power consumption. The short-circuit current which is due to the DC path between the supply rails during output transitions. $P_{leakage}$ is the leakage power.

With supply voltage scaling down, the threshold voltage also gets reduced which leads to the exponential growth of the sub-threshold leakage current. The diode leakage is typically 1 picoA for a 1 micro-meter minimum feature size. The sub threshold leakage current for long channel devices increases linearly with the ratio of the channel width over channel length and decreases exponentially with V_{GS}-V_t where V_{GS} is the gate bias and V_t is the threshold voltage. Sub threshold leakage is the dominant leakage now. As gate oxide get thinner, gate leakage may become the dominant part even in the future. $P_{leakage} = I_{leakage} * V_{dd}$. The leakage current, is determined by the fabrication technology, which has two components: 1) Reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor, and 2) The sub-threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage. Leakage currents in CMOS circuits can be made small with proper choice of device technology. Another source of power dissipation is the standby current which is the DC current drawn continuously from V_{dd} to ground and the capacitance current which flows to charge and discharge capacitive loads during transition of the logic. Standby currents are important only in CMOS design styles like pseudo-nMOS and nMOS pass transistor logic. The static power dissipation refers to the sum of leakage and standby dissipations.

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III. AN OVERVIEW OF DIFFERENT POWER OPTIMIZATION DESIGNS

A. TBHEX Architecture

Due to its widespread applications in *mobile*, and other portable computing and communications services low power video codec chip is highly on demand. Motion estimation is the most important task [12] in the total video coding process, which consumes major portion of power. So low power VLSI architecture for the motion estimation block is considered [1]. For motion estimation modification of Hexagonal block matching algorithm (BMA) has been adopted in which TBHEX (Threshold-based Hexagonal BMA) has an inherent property of less computational complex, faster throughput, regular data flow and possible to realize with minimum functional blocks [1]. This low power architecture based on TBHEX BMA is termed as TBHEX architecture. By using two on-chip memories (MEMR and MEMC) [1] the total number of external memory accesses is reduced approximately 88.88%, which in turn reduces the switching activity of the external memory access and thus reduces 88.88% of total switching power dissipated for accessing external memory. The experimental result shows that proposed TBHEX architecture requires only 22.14 mW [1]. Power requirement in TBHEX is 49.47% less than [5]

B. Efficient Carry Generation Technique Incorporating Energy Recovering Logic Circuitry for low power VLSI

In past few years several approaches have been developed to improve Power metric. Adiabatic Logic is a powerful contrivance in growing low power domain which performs computation in reversible manner which leads to zero energy consumption with the use of AC Power supply. A carry generation logic circuit for adders has been proposed [2] which shows improvement in power consumption, by taking adiabatic logic into account. Adder has been designed in 90nm TSMC Technology at operating frequency of 10MHz which shows 76.2% improvement in energy consumption while compared with conventional design [2].

C. Circuit Level Low Power Design

1) Dynamic Power Reductions:

From power consumption equation given in [3], there are numerous ways to lower the power consumption. As clocking system is the dominant contributor of the total dynamic power dissipation due to the fact that it has the largest fan-out, highest switching activity (100%), and largest length, low power design techniques for clocking system are reviewed. These include reducing supply voltage, double edge triggering, and reducing redundant switching.

2) Leakage Control: As feature size shrinks with scaling, the leakage current increases rapidly, the MTMOS technique as well as transistor stacking, dynamic body biasing and supply voltage ramping could be used to reduce leakage standby power consumption [4]. The main trade offs are between standby power, invocation overhead, area cost, and runtime performance impact. The major challenge is to ensure that a module is placed in the appropriate standby mode when needed [10].

D. Design of Combinational Circuits by Cyclic Combinational Method for Low Power VLSI

An useful technique is to design the combinational part of any circuit in cyclic way for low power VLSI design. Combinational circuits are generally considered as acyclic structured. The main aim of cyclic circuit is to introduce structural feedback & to avoid the logical feedback in order to get combinational primary output. The study of cyclic circuit

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includes functional analysis and the timing analysis**.** Cyclic circuits introduces structural feedback in the circuits which indeed increases the no. of effective input variables in the circuit & provides greater flexibility in producing minimized Boolean expression of the primary outputs. Cyclic circuits can produce same result as acyclic combinational circuits with lesser no of gates [6]. That means cyclic circuits are better in area, power consumption and delay consideration compared to conventional acyclic circuit. A practical implementation with small runtimes for different practical circuits demonstrates the efficacy of this algorithm [6].

E. Power Gating designs in Low Power VLSI Circuits

The most trustful approache to low power design is "Power Gating" for which analysis is done in [7]. The focus is made on CMOS devices in nanometer scale technology which is being the most adopted in current VLSI systems. In a power gating structure, a transistor with high threshold voltage (V_{th}) is placed in series with a low V_{th} device, the high V_{th} transistor is called as the Sleep Transistor [7]. In the power gating structure, a circuit operates in two modes. In the active mode, the sleep transistors are turned ON and can be treated as the functional redundant resistances. In the sleep mode, the sleep transistors are turned OFF to reduce the leakage power [7].

Optimum sleep transistor designs are very critical for a successful power-gating design. In the power gating, sleep transistors are used as switches to shut off power to parts of a design in standby mode. While implementing sleep transistors in CMOS circuits, the performance is found to be better when they are interconnected to form a network [7]. Among the leakage reduction techniques, the power gating technique has become one of the most effective methods. With the circuit density being increased at nanoscale, the scheduling of the sleep transistors plays a vital role in reducing the leakage power of the circuit. The power gating design is more efficient than the DSTN circuits designed at 65nm scale [7].

F. Geometric and Non-Linear Programming as Optimization Algorithms for low power VLSI

Generally, two kinds of algorithms can be used for optimization of effective parameters in Low Power VLSI circuits that are Linear and Nonlinear Programming. LP modeling is widely used because LPs can be solved with great reliability and efficiency. NLP modeling is relatively easy, since the objective and constraint functions can be any nonlinear functions. NLP in the low power design has frequently been utilized, due to its high speed and reasonable reliability. On the other hand though, the well developed and already known GGP algorithm became then important because of two recent developments: 1) New solution methods could solve even large-scale GPs extremely efficiently and reliably [8] like NLP and 2) It was found that many practical problems, especially in electrical circuit design, are equivalent GGPs [9].

GGP modeling can be much more difficult than NLP, because objective and constraint functions must be considered. Solving a GGP is easier as compared to solving a general NLP as it needs some compromise like accepting a local rather than a global solution [8]. GGP method only requires the designer to mathematically model the circuit in its special problem format. In logic level of abstraction, the proposed procedure in [11] based on Logical Effort method and GGP algorithm, exhibited high precision and acceptable speed compared to NLP algorithms.

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G. Clock Gating

Clock gating is one of the power-saving techniques used on the Pentium 4 processor and in next generation processors. To save power, clock gating refers to activating the clocks in a logic block only when there is work to be done. There are various clock gating techniques that can be used to optimize power in VLSI circuits at RTL level. In order to achieve their power budgets designers go through several iterations to optimize power. Clock power consumes 50-70 percent of total chip power and is expected to significantly increase in the next generation of designs at 45nm and below as power is directly proportional to voltage and the frequency of the clock as shown in the following equation:

$$\text{Power} = \text{Capacitance} * (\text{Voltage})^2 * (\text{Frequency})$$

Hence, reducing clock power is very important. RTL Clock Gating is the most commonly used optimization technique for reducing dynamic power. The clock gating is discussed in [13]. The challenge of optimizing power by adding clock gating is knowing where and when to insert clock gating. Hardware designers use clock gating to turn off inactive sections of the design and reduce overall dynamic power consumption. The RTL approach is important because designers usually verify power only at the gate level and any change to the RTL needs many design iterations to reduce power.

H. Low Power VLSI Circuit Implementation using Mixed Static CMOS and Domino logic with Delay Elements

The advent of dynamic CMOS logic, more precisely domino logic, made them widely used for the implementation of low power VLSI circuits. However, the main drawback of this logic is the non implementation of inverted logic. In order to implement the inverted logic, it is required to duplicate the logic circuit up to that part with inverted inputs which results in increase in area, delay as well as the power dissipation of the circuit. On the other hand, it is very simple to realize the circuit with both the inverted and non-inverted logic using static CMOS implementation. This problem is addressed with the realization of the circuit which requires the implementation of inverted logic using mixed static and domino logic in [14] in which implementation of high fan-in NAND gate cascaded with AND gate is considered. With the comparison of all the three logics with a fixed fan-in of 7, 8 and 9 for both the gates, on an average 69.7% improvement is achieved in Power Delay Product (PDP), 11.4% improvement in area in terms of transistors using mixed logic implementation over static logic implementation and 68.64% improvement in PDP and 28.4% improvement in area over dynamic CMOS implementation when designed in 180nm technology [14]. The model in [14] can be applied for implementation of any intermediate inverted logic and it need not be a strict domino gate – static gate – domino gate and this can be extended for implementing not only an inverter but also other inverting gates.

I. Asynchrobatic Logic for low power VLSI Design

Depending upon the application, there are numerous methods that can be used to reduce the power consumption of VLSI circuits, these can range from low-level measures to high-level measures .The two that motivated the investigation were asynchronous logic [15] & [16] and adiabatic logic [17]. These two technologies have been combined to create an Asynchronous, Adiabatic Logic methodology, called *Asynchrobatic* Logic [18]. The name is derived as a concatenation and shortening of Asynchronous, Adiabatic Logic. One of the properties of asynchronous systems that make them useful in these applications are that

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circuits include a built-in insensitivity to variations in power supply voltage, with a lower voltage resulting in slower operation rather than the functional failures that would be seen if traditional synchronous systems were used.

Another major advantage is the fact that when an asynchronous system is idle there will be no ticking clock signals, whereas in synchronous systems, these clock signals are propagated throughout the entire system and convert energy to heat, without performing any useful computations. Adiabatic logic is focused on issues associated with the thermodynamics of computation. *Asynchrobatic* Logic was born out of idea to attempt to find a way to unify the low power benefits from these fields. The ability to implement the GCD circuit is a major achievement, as it proves that *Asynchrobatic* Logic can be use to implement complex systems that include decision and iteration.

J. Sleepy Keeper: For Low-leakage Power VLSI Design

Scaling down of the CMOS technology feature size and threshold voltage for achieving high performance has resulted in increase of leakage power dissipation. A new approach, named "sleepy keeper", reduces leakage current while saving exact logic state. Sleepy keeper uses traditional sleep transistors plus two additional transistors – driven by a gate's already calculated output – to save state during sleep mode. Dual V_{th} values can be applied to sleepy keeper to reduce sub-threshold leakage current. Sleepy keeper achieves leakage power reduction with the advantage of maintaining exact logic state (instead of destroying the logic state when sleep mode is entered). Based on experiments with a 4-bit adder circuit, sleepy keeper approach achieves up to 49% less delay and 49% less area than the sleepy stack approach. The sleepy keeper technique results in ultra low static power consumption with state saving.

IV. CONCLUSION

- The designing for low power has added another dimension to the already complex design problem and the design has to be optimized for power as well as performance and area.
- Low power design requires a rethinking of the conventional design process, where power concerns are often overridden by performance and area considerations.
- In this paper we have reviewed low-power design principles, an overview of different low power design methodologies and techniques ranging from technology and devices to circuits and systems.

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