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STUDY OF PHASE LOCKED LOOP FREQUENCY SYNTHESIZER

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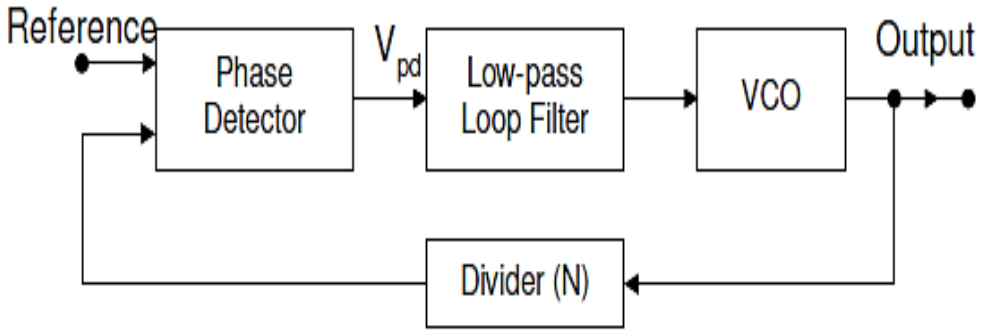
Abstract: A phase-locked loop is a feedback control system that maintains a constant phase angle relative to a reference signal. Phase locked loop (pll) is widely used in frequency synthesis applications. There are two most popular phase locked loop frequency synthesizer architecture viz. Integer n frequency synthesizer and fractional n frequency synthesizer. Frequency synthesis application of pll is studied using both the architecture and they are compared theoretically and also by performing simulations. The main scope of this research work will be trying to reduce the output phase noise in integer n and fractional n frequency synthesizer while achieving wider bandwidth of operation.

I. INTRODUCTION

The advancement In Modern Communication Has Been Possible Due To Continuous Work Done To Improve Communication Blocks. Frequency Synthesis Block is a Major Block in Communication System. Function of frequency synthesis block is to generate frequencies between certain ranges. Frequency generated is used to up convert or down convert a transmitted or received signal respectively. Phase Locked Loop is a feedback Control System and maintains a constant phase relative to input reference signal. Phase-locked loops can be used to generate, stabilize, modulate, demodulate a signal from a "noisy" communications channel and it can be used to generate stable output high frequency signals from a fixed low-frequency signal.



Phase Locked Loop Block Diagram

- **Phase detector:**
  The phase detector compares the phase of the reference signal and the phase of the output signal. It produces an error signal which is proportional to the phase difference of its two input signals.

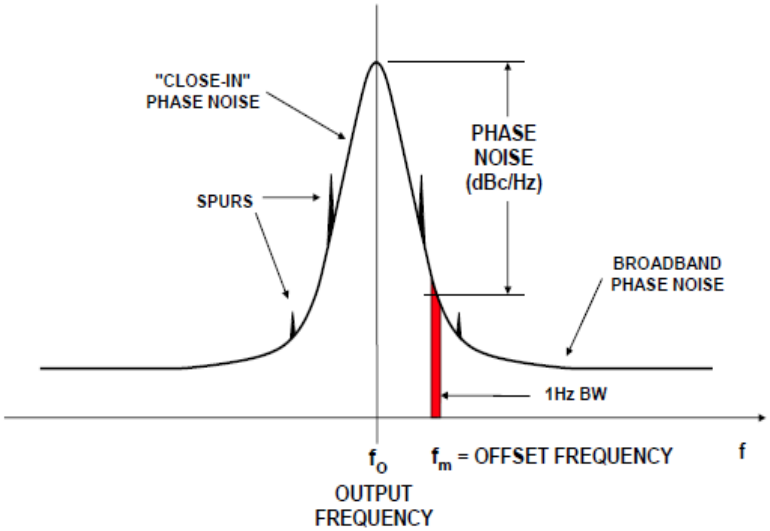
- **Low pass filter :**
  The output of pd is filtered to suppress the high frequency components and then is applied to the oscillator as a controlling signal (voltage or current). The most important characteristics of a PLL, such as loop bandwidth, settling time, and phase noise are highly dependent on loop filter design. , The loop filter can be realized either with pure passive elements or with an operational amplifier to form an active loop filter.

- **Voltage controlled oscillator (vco):**
  Voltage controlled oscillator is a circuit which generates periodic signal whose frequency is the function of input voltage to the vco. A VCO is a voltage controlled oscillator, its output frequency ω_0 is linearly proportional to the control voltage V_c which is generated by the Phase detector.

- **Divider:**
  The functionality of this block is to divide the oscillator frequency by a factor *n*. In this configuration the vco output frequency will be equal to *n* times the reference frequency.

II. PHASE NOISE

The frequency broadening caused by random noise fluctuations due to device noise such as flicker noise, shot noise and thermal noise is termed as Phase noise. Power Supply and VCO are two main source of Phase Noise. The phase noise spectrum shows the noise power in a 1 Hz bandwidth as a function of frequency. Calculation of phase noise as the ratio of the noise in a 1 Hz bandwidth at a specified frequency offset, f_m, to the oscillator signal amplitude at frequency f_o and It is expressed in dBc/Hz.



Phase Noise and Spurious Frequencies at PLL Output

The ratio between the powers at a frequency offset (f_o) within a certain bandwidth to the power of the center frequency (f_c), is defined as a phase noise. Phase Noise can be modelled as some constant that is multiplied by the closed loop transfer function. The closed loop transfer function can be approximated by the N divider value, provided that the offset frequency is within the loop bandwidth. Since phase noise is caused by a noise voltage, the

noise power would be proportional to N^2, hence this implies that phase noise varies as 20log (N). Phase noise floor is this constant value and calculated as

$$Phase\ nois(offset) = \frac{\approx \text{PhaseNoiseFloor} + 20\log N}{\text{PhaseNoiseFloor} + 20\log \text{CLT(offset)}}$$

- **Spurious Frequencies (Spurs):**

  A spur is the non-harmonic discrete frequency tone. Spur in PLL result from the FM modulation by the VCO due to VCO is naturally a voltage-to-frequency converter. Spurs signals occur due to the current mismatch in the charge pump and glitches on the voltage control line.

III. METHODOLOGY

- ***Integer n frequency synthesizer***

A simple Integer N frequency Synthesizer is shown in Figure. Its output is simply N times the F_{ref} frequency. Divider N count can be changed to get various output frequencies.

$$F_{out} = NF_{ref}$$

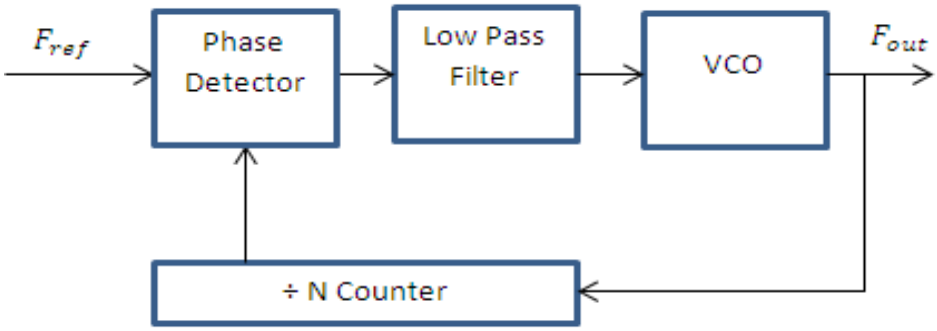
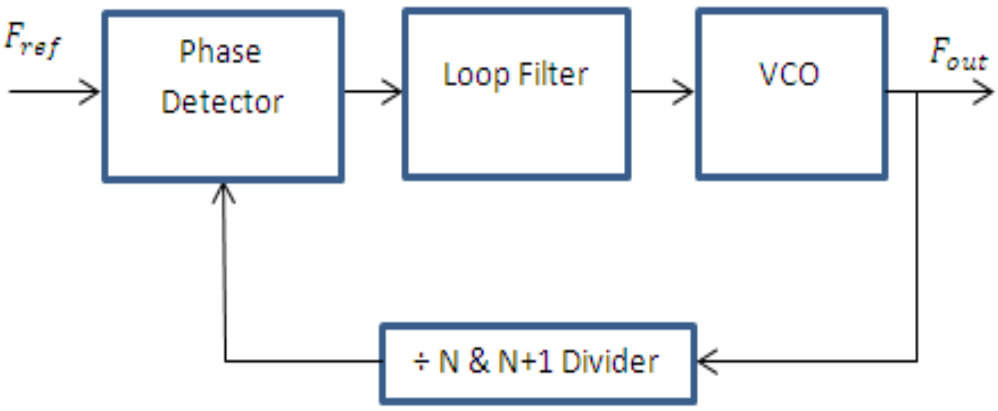


Figure: Integer N Frequency Synthesizer

- **Fractional n frequency synthesizer**

Fractional-n allows the resolution at the pll output to be reduced to small fractions of the PFD. Fractional -n frequency synthesizer uses the technique of alternating between the division of VCO output by n and n+1 and thus achieving division by a fraction.



Fractional N Frequency Synthesizer Block Diagram.

IV. CONCLUSION

Two most widely used pll frequency synthesizer architectures namely integer n and fractional n frequency synthesizers has designed to reduce phase noise.

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